

Abstract

1 A solid state imager with pixels arranged in columns and rows has the pixels
2 are configured into groups of at least a first pixel and a second pixel, each said
3 group sharing a pixel output transistor having a sense electrode and an output
4 electrode and a reset transistor having a gate coupled to receive a reset signal and an
5 output coupled to the sense electrode of the associated shared pixel output
6 transistor. Each of the pixels has a photosensitive element whose output electrode
7 is coupled to the sense electrode of the shared pixel output transistor and a gate
8 electrode coupled to receive respective first and second pixel gating signals. This
9 configuration reduces the number of FETs to two transistors for each pair of pixels,
10 and also can achieve true correlated double sampling correction of FPN.